No. 5,536,958) under 35 U.S.C. §103(a). The Examiner also rejects the Specification for lacking appropriate headings.

Applicants have amended the Specification to add proper headings, and believe the objection to the Specification has been thus overcome. Applicants have also amended claims 6 and 10 to better define the invention and to overcome the language deficiencies, and have also added new set of product claims 11-20 which are directed to the semiconductor device of the present invention. Applicants respectfully traverse the rejections of the Examiner based on the above amendment and detailed explanations as follows:

First of all, applicants believe a brief explanation of the present invention will be helpful in understanding the patentably distinguishing feature of the present invention over the cited prior art. The present invention teaches a semiconductor device with a novel arrangement by which the saturation degree is limited while the device has a good reproducibility in leakage current and therefore is suitable for mass manufacture. In particular, as taught in the present invention, a partial region of the second semiconductor region (base region), which lies outside the third semiconductor region (emitter region) and adjacent the second connection conductor, has a smaller flux of dopant atoms than other part of the second semiconductor region, whereby the partial region together with the subjacent portion of the collection region forms a base diode which acts as a pn clamping diode for limiting saturation degree in the device (see, for example, page 5, lines 5-10). Therefore, unlike in the prior art such as Baliga cited in the Specification as well as by the Examiner, no Schottky clamping diode, which is too variable in leakage current, is needed in the semiconductor device of the present invention. Thus, the semiconductor device of the present invention has a narrow spread and a good reproducibility as regards its leakage current (see, e.g., page 3, lines 4-7) . The above emphasized feature is expressly defined in the added independent claim 11 for the inventive semiconductor device, and is also defined in similar language in the amended independent claim 6 for a method for manufacturing the semiconductor device. To realize a smaller flux of dopant atoms, the

partial region may be formed with either a smaller thickness or a lower doping concentration, or both, as defined in the dependent claims 7-8 and 12 -16.

Applicants do not believe that the present invention as defined in independent claims 6 and 11 is obvious over Baliga or Shen or their combination as neither of the cited patents discloses or implies the above emphasized distinguishing feature.

Baliga, which is also cited by applicants as prior art in the present application, discloses a bipolar transistor device that includes an integral antisaturation Schottky diode resulting from direct contact between the base electrode and the collector region. There is no teaching in Baliga that the base region has a smaller flux of dopant atoms in a partial region outside the emitter region. To the contrary, as shown throughout the drawings in Baliga, the base region has a smaller thickness at the emitter region, which implies a higher flux of dopant atoms if the doping concentration is consistent in the whole base region.

Shen teaches a semiconductor device having an improved high voltage protection scheme that comprises an integrated Schottky diode in conjunction with a plurality of back to back diodes to limit voltage between the gate and the drain. Shen, however, does not teach that the base region (gate) has a smaller flux of dopant atoms in a partial region outside the emitter region (source). This feature cannot be found in the embodiment described in col. 5, line 6 ▮ col. 6, line 15 and shown in Figure 5 or anywhere else in Shen. To the contrary, as clearly shown in Figure 5, the second semiconductor region (pinch-off structures) 42 has a consistent thickness, which implies a consistent flux of dopant atoms at the same doping concentration. Besides, applicants believe that the Examiner has improperly misread the depletion region 51 (which is of the first conductivity type, i.e., the same conductivity type of the drain) as the second semiconductor region, the high voltage clamping device 45 as the partial region of the second semiconductor region, and the electrical contact 44 (which connects between the contact region 43 and one end of a chain of polysilion diodes 46) as the second conductor in the present invention.

Therefore, applicants believe that independent claims 6 and 11 are not obvious over the cited patents, and are therefore patentable. At least for the same reason, dependent claims 7-10 and 12-20, each of which includes all the limitations in either claim 6 or claim 11, are also patentable. In particular, claims 7-8 and 12-16 further defines that the partial region is formed with either a smaller thickness or a lower doping concentration, or both. Claim 10 and 19-20 further defines that the device comprises a fourth semiconductor region of the first conductivity type which is present between the partial region of the second semiconductor region and the second connection conductor. These features are also not disclosed or taught in either Baliga or Shen, and therefore further strengthen the patentability of these dependent claims.

Applicants therefore respectfully request reconsideration and allowance in view of the above remarks and amendments. The Examiner is authorized to deduct additional fees believed due from our Deposit Account No. 11-0223.

Respectfully submitted,

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Dated: December 4, 2002

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(Reg. No. 34,356)

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal service as first class mail, in a postage prepaid envelope, addressed to Box Non-Fee Amendment, Commissioner for Patents, Washington, D.C. 20231 on December 4, 2002.

Dated December 4, 2002 Signed Paula M. Halsey Print Name Paula M. Halsey

MARKED-UP VERSION OF THE AMENDED

6. (Twice amended) A method of manufacturing a semiconductor device [whereby a first semiconductor region is formed in a semiconductor body comprising a substrate, which first semiconductor region lies in the semiconductor body, is of a first conductivity type, forms a collector region of a bipolar transistor, and is provided with a first connection conductor, whereby a second semiconductor region of a second conductivity type opposed to the first is formed above said first semiconductor region, which second semiconductor region forms a base region of the transistor, adjoins the surface of the semiconductor body, and is provided with a second connection conductor at said surface, and whereby a third semiconductor region is formed which is recessed into the second semiconductor region, which is of the first conductivity type, which forms an emitter region of the transistor, and which is provided with a third connection conductor, and whereby the device is provided with means for preventing a saturation of the transistor during normal use, characterized in that the second semiconductor region for preventing a saturation of the transistor, and in that a partial region of that portion of the second semiconductor region which lies outside the third semiconductor region, as seen in projection, and adjacent the second connection conductor is provided with a smaller flux of dopant atoms.] which comprises a first semiconductor region of a first conductivity type with a first connection conductor forming a collector region of a bipolar transistor, a second semiconductor region of a second conductivity type opposed to the first conductivity type with second connection conductor, forming a base region of the transistor, and a third semiconductor region of the first conductivity type with a third connection conductor forming an emitter region of the transistor; said method comprising:

providing a substrate of the first conductivity type, and forming thereon an epitaxial layer of the first conductivity type to form the first semiconductor region;

forming the second semiconductor region on the first semiconductor region, the

second semiconductor region having a partial region with a smaller flux of dopant atoms than other part of the second semiconductor region;

forming the third semiconductor region which lies recessed in the other part of the second semiconductor region; and

providing first, second and third connection conductors to the first, second and third regions with a connection conductor respectively, wherein the second conductor is adjacent to the partial region of the second semiconductor region.

10. (Twice Amended) A method as claimed in claim 6, characterized in that a [thin, strongly doped] fourth semiconductor region of the first conductivity type is formed between the partial region of the second semiconductor region and the second connection conductor [, preferably] simultaneously with the third semiconductor region.